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PATENT ABSTRACTS OF JAPAN

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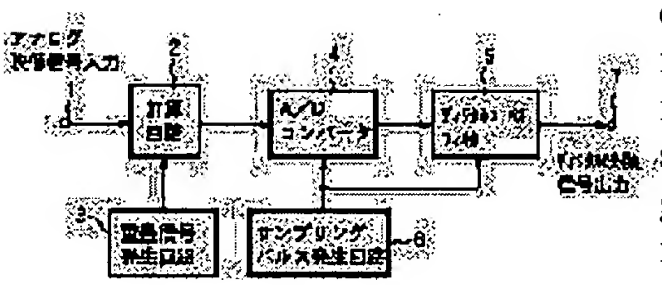
(54) A/D CONVERTING CIRCUIT



(57)Abstract:

PURPOSE: To enable analog/digital(A/D) conversion while reducing quantizing errors even concerning a signal over a wide frequency band like a video signal.

CONSTITUTION: A sampling pulse generating circuit 6 generates a sampling pulse whose frequency is higher than the double peak frequency of an input video signal. A superimposing signal generating circuit 3 generates a superimposing signal, whose frequency is lower than the 1/2 frequency of the sampling pulse but higher than the peak frequency of the input video signal, having a fixed amplitude and this superimposing signal is added to the input video signal by an adder circuit 2. An A/D converter 4 converts the output signal of the adder circuit 2 to a digital signal based on the sampling pulse. A digital low-pass filter 5 attenuates the component of the superimposing signal from the output digital signal of the A/D converter 4 and outputs the result to an output terminal 7.

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CLAIMS

[Claim(s)]

[Claim 1] On the frequency of the sampling pulse generating circuit which generates a sampling pulse twice [more than] the frequency of the highest frequency of an input signal, and the 1 / 2 double less or equal of this sampling pulse And the superposition signal generating circuit which generates the superposition signal of the fixed amplitude on a frequency higher than the highest frequency of said input signal, The A/D-conversion circuit characterized by having an adder circuit adding said input signal and said superposition signal, and the A/D converter which changes the output signal of this adder circuit into a digital signal based on said sampling pulse.

[Claim 2] Said A/D converter is an A/D-conversion circuit according to claim 1 characterized by being the configuration of changing an input signal into a digital signal by dividing into two, a high order bit and the remaining lower bits.

[Claim 3] The A/D-conversion circuit according to claim 1 characterized by having further the digital low pass filter which decreases said superposition signal component from the output digital signal of an A/D converter.

[Claim 4] Said superposition signal generating circuit is [claim 1 characterized by generating said superposition signal which synchronized with this sampling pulse based on said sampling pulse thru/or] an A/D-conversion circuit given in any 1 term among 3.

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] This invention relates to the A/D-conversion circuit which starts an A/D-conversion circuit, especially carries out analog-to-digital conversion of the video signal.
[0002]
[Description of the Prior Art] Although the A/D-conversion circuit which changes an analog signal into a digital signal is used widely conventionally, since the frequency band of a video signal is a broadband comparatively, as for the A/D-conversion circuit which changes a video signal into a digital video signal, high speed is required comparatively. For this reason, as an A/D-conversion circuit for images, it is A/D-conversion ********** of all parallel connected types conventionally.
[0003] When obtaining the resolving power of N bit, the A/D-conversion circuit of all these parallel connected types The comparator of a bit (2N-1), Two or more partial pressure resistance which generates mutually different reference voltage for making each of two or more of these comparators compare with an input video signal, It consists of encoders for changing the output digital signal of two or more comparators into the binary code of N bit. A level comparison is separately carried out at coincidence with the reference voltage which corresponds with two or more comparators of the above [an input video signal], and an output digital signal is acquired by letting an encoder pass for the comparison result. The A/D-conversion circuit of all these parallel connected types has the features that the precision of differential 1 quantization is comparatively good, at high speed.
[0004] Moreover, the so-called 2 step flash plate mold A/D-conversion circuit changed as other conventional A/D-conversion circuits by dividing into two, high order two or more bits and the remaining bits, is known. The 1st comparator of the plurality [circuit / this / conventional / A/D-conversion] for high order two or more bits, Two or more 2nd comparators for lower bits, and a reference voltage generating means to input the reference voltage of mutually different level into the 1st and 2nd comparators, It consists of a means for switching which switches the reference voltage impressed to the 2nd comparator according to the output of the 1st comparator, and an encoder which changes each output of the 1st and 2nd comparators into the digital signal of the predetermined number of bits, respectively.
[0005] According to this conventional A/D-conversion circuit, an input video signal is inputted into two or more 1st and 2nd comparators at juxtaposition, respectively, first step compares the 1st comparator and reference voltage by the side of a high order, the reference voltage to the 2nd comparator by the side of low order is switched according to the above-mentioned comparison result at the second step, and the 2nd comparator performs the comparison with an input video signal. And the digital signal of high order two or more bits and the digital signal of low order two or more bits are acquired with the encoder formed by corresponding, respectively in each comparison output of the 1st and 2nd comparators obtained by doing in this way.
[0006]
[Problem(s) to be Solved by the Invention] However, among the above-mentioned

conventional A/D-conversion circuits, the thing of the former configuration has the problem that power consumption is size while a circuit scale becomes large since the comparator of about 1024 (= 210) individual and the partial pressure resistance for reference voltage generating are needed when it is going to output a 10-bit digital video signal.

[0007] Moreover, among the above-mentioned conventional A/D-conversion circuits, the thing of the latter configuration has the problem that the error in the knot of the digital signal output of a high order and a low-ranking digital signal output is large, while there are few comparators, and there are little circuit scale and power consumption and they end.

[0008] In for example, the case of a configuration of dividing into 6 bits of high orders and 4 bits of low order, and obtaining a digital signal output The property of an output digital signal over an input analog signal comes to be shown in drawing 4 , and although it is good since change of the quantization 1 Width of face from "0000001110" to "0000001111" is only change of 4 bits of low order, a 10-bit output Since the change of quantization 1 Width of face to "0000010000" from "0000001111" is change by the knot accompanied by change of 6 bits of high orders, and 4 bits of both low order, as A shows to this drawing, the problem of being inaccurate (distortion being large) has it.

[0009] that by which this invention was made in view of the above point -- it is -- a video signal -- like -- the signal of a wide band -- also receiving -- a quantization error -- it aims at offering the A/D-conversion circuit which can carry out analog-to-digital conversion few.

[0010]

[Means for Solving the Problem] In order to attain the above-mentioned purpose, this invention is the frequency of the sampling pulse generating circuit which generates a sampling pulse twice [more than] the frequency of the highest frequency of an input signal, and the 1 / 2 double less or equal of a sampling pulse. And the superposition signal generating circuit which generates the superposition signal of the fixed amplitude on a frequency higher than the highest frequency of an input signal, It considers as the configuration which has an adder circuit adding an input signal and a superposition signal, and the A/D converter which changes the output signal of an adder circuit into a digital signal based on a sampling pulse.

[0011]

[Function] In this invention, since analog-to-digital conversion is carried out by the A/D converter to an addition composite signal with the superposition signal of high frequency and he is trying to generate a digital signal rather than an input signal and this, change of digital value (sampling value) can be made small rather than it carries out direct analog-to-digital conversion to an input signal.

[0012] Moreover, a superposition signal can be reduced by having further the digital low pass filter which decreases a superposition signal component from the output digital signal of an A/D converter, and can acquire a desired digital signal.

[0013]

[Example] Next, the example of this invention is explained. Drawing 1 shows the block diagram of one example of this invention. Among this drawing, after the analog video signal inputted into the input terminal 1 is supplied to an adder circuit 2 and added with the superposition signal from the superposition signal generating circuit 3 here, it is

supplied to A/D converter 4 and changed into a digital signal based on the sampling pulse from the sampling pulse generating circuit 6.
[0014] This A/D converter 4 is the so-called 2 step flash plate type better known than before of A/D converter, as described above, as compared with reference voltage which is mutually different in two or more comparators for high order bits in an input composite signal, according to that comparison result, it switches reference voltage, impresses it to two or more another comparators for lower bits, compares this reference voltage with the above-mentioned input composite signal, and repeats the same actuation as the following at the second step by first step. And the digital value of remaining low order two or more bits is outputted for each output which outputted the digital value of high order two or more bits through the encoder for high order bits, and was taken out from two or more comparators for [above] lower bits in each output taken out from two or more comparators for [above] high order bits through the encoder for lower bits.
[0015] Here, the frequency of a sampling pulse is 14.3MHz which is twice [more than] the frequency of the highest frequency of the input analog video signal which it is going to pass from the sampling theorem of nyquist, and is 4 times the frequency of the chrominance-subcarrier frequency of for example, an input analog video signal here. Moreover, the above-mentioned superposition signal is a sine wave 1/2 twice the frequency of the frequency of this sampling pulse, and the amplitude is about 5 times of 1 quantization width of face.
[0016] Thus, from A/D converter 4, the composite signal of a video signal and a superposition signal is changed into a digital signal by dividing into two, a high order bit and a lower bit, as a whole, it is taken out by 10 bits and a quantifying bit number is supplied to the low pass filter 5 this digital signal of whose is a digital filter which is operating synchronizing with the sampling pulse from the sampling pulse generating circuit 6. It is low frequency from a superposition signal, and rather than the highest frequency of an input analog video signal, since cut-off frequency is set as 6MHz of a high frequency, it decreases a superposition signal by carrying out the passage output of the video-signal component as it is to an output terminal 7, and this digital low pass filter 5 is not outputted to an output terminal 7.
[0017] Drawing 2 shows an example of an input signal wave of A/D converter 4. As shown in this drawing, the superposition signal II from the above-mentioned superposition signal generating circuit 3 is compounded in an adder circuit 2 to the input video signal I which carries out the increment in monotone, and if the composite signal is sampled to the timing shown in drawing 2 by the arrow head by the above-mentioned sampling pulse in A/D converter 4, the sampling point will serve as a location shown in drawing 2 by the black dot. Therefore, also in the big input level of the quantization error of A/D converter 4, since it becomes the average with the level which the sampling value before and behind the level left for a while, a quantization error decreases.
[0018] Next, other examples of this invention are explained. Drawing 3 shows the block diagram of other examples of the A/D-conversion circuit which becomes this invention. The same sign is given to the same component as drawing 1 among this drawing, and the explanation is omitted. In drawing 3 , the analog video signal with a highest frequency of about 6MHz inputted from the input terminal 1 is supplied to adder 2a in an adder circuit 2 through the low pass filter (LPF) 10 whose cut-off frequency is 14MHz.
[0019] On the other hand, the sampling pulse generating circuit 12 is supplied to the

superposition signal generating circuit 13 while it generates the 28.6MHz sampling pulse which synchronized with the synchronization pulse from an input terminal 11 and supplies this sampling pulse to A/D converter 4 and the digital low pass filter 14, respectively.

[0020] The superposition signal generating circuit 13 is 14.3MHz of the 1/2 twice as many frequency which synchronized with the input sampling pulse as this, and as the amplitude described above, generates the superposition signal of 5 quantization width-of-face extent, supplies it to adder 2a, and it makes it add with the analog video signal from LPF10 here.

[0021] After the composite signal of the analog video signal and superposition signal which were taken out from this adder 2a is amplified with amplifier 2b, it is supplied to A/D converter 4, and over sampling technique is carried out by the 28.6MHz sampling pulse, for example, it is changed into a digital signal with a quantifying bit number of 10 bits. With the digital low pass filter 14 whose passband of this digital signal is about 6MHz, it passes as it is, and a video-signal component is outputted to an output terminal 7, and decreases a superposition signal component. Since this example can sample the crest of a superposition signal, and the part of a trough to accuracy, respectively since the superposition signal synchronizes with a sampling pulse, and they are carrying out over sampling technique, it is more exact and can be changed into a digital signal with few quantization errors.

[0022] In addition, although this invention is not limited to the above-mentioned example and the digital low pass filters 5 and 14 for superposition signal attenuation were formed in the A/D-conversion circuit in the example, it is also possible to attenuate a superposition signal with the filter prepared in the D/A conversion circuit which follows. Moreover, a superposition signal may be the frequency of under 1 / 2 double of the frequency of a sampling pulse, and may be a frequency higher than the highest frequency of an input signal (you may not be a video signal).

[0023]

[Effect of the Invention] By according to this invention, carrying out analog-to-digital conversion by the A/D converter to an addition composite signal with the superposition signal of high frequency, and generating a digital signal rather than an input signal and this, as explained above Since change of digital value (sampling value) can be made small rather than it carries out direct analog-to-digital conversion to an input signal, Can acquire the digital signal which reduced the differential-quantization error compared with the former, and therefore, since the A/D converter of a configuration of changing by dividing into two, high order two or more bits and the remaining bits, can be used Power consumption can also be reduced while being able to reduce a circuit scale compared with the A/D-conversion circuit of all parallel connected types.

TECHNICAL FIELD

[Industrial Application] This invention relates to the A/D-conversion circuit which starts an A/D-conversion circuit, especially carries out analog-to-digital conversion of the video signal

PRIOR ART

[Description of the Prior Art] Although the A/D-conversion circuit which changes an analog signal into a digital signal is used widely conventionally, since the frequency band of a video signal is a broadband comparatively, as for the A/D-conversion circuit which changes a video signal into a digital video signal, high speed is required comparatively. For this reason, as an A/D-conversion circuit for images, it is A/D-conversion ********** of all parallel connected types conventionally.

[0003] The A/D-conversion circuit of all these parallel connected types is the comparator of a bit (2N-1), when obtaining the resolving power of N bit, It consists of two or more partial pressure resistance which generates mutually different reference voltage for making each of two or more of these comparators compare with an input video signal, and an encoder for changing the output digital signal of two or more comparators into the binary code of N bit, and a level comparison is separately carried out at coincidence with the reference voltage which corresponds with two or more comparators of the above [an input video signal], and an output digital signal is acquired by letting an encoder pass for that comparison result. The A/D-conversion circuit of all these parallel connected types has the features that the precision of differential 1 quantization is comparatively good, at high speed.

[0004] Moreover, the so-called 2 step flash plate mold A/D-conversion circuit changed as other conventional A/D-conversion circuits by dividing into two, high order two or more bits and the remaining bits, is known. This conventional A/D-conversion circuit is two or more 1st comparators for high order two or more bits, It consists of a reference voltage generating means to input two or more 2nd comparators for lower bits, and the reference voltage of mutually different level into the 1st and 2nd comparators, a means for switching which switches the reference voltage impressed by the 2nd comparator according to the output of the 1st comparator, and an encoder which changes each output of the 1st and 2nd comparators into the digital signal of the predetermined number of bits, respectively.

[0005] According to this conventional A/D-conversion circuit, an input video signal is inputted into two or more 1st and 2nd comparators at juxtaposition, respectively, first step compares the 1st comparator and reference voltage by the side of a high order, the reference voltage to the 2nd comparator by the side of low order is switched according to the above-mentioned comparison result at the second step, and the 2nd comparator performs the comparison with an input video signal. And the digital signal of high order two or more bits and the digital signal of low order two or more bits are acquired with the encoder formed by corresponding, respectively in each comparison output of the 1st and 2nd comparators obtained by doing in this way

EFFECT OF THE INVENTION

[Effect of the Invention] As explained above, in this invention, rather than an input signal and this, analog-to-digital conversion is carried out by the A/D converter to an addition composite signal with the superposition signal of high frequency, and a digital signal is generated. Therefore, the digital signal which reduced the differential-quantization error

compared with the former since change of digital value (sampling value) was made small rather than it carries out direct analog-to-digital conversion to an input signal can be acquired, and power consumption can also be reduced while being able to reduce a circuit scale compared with the A/D-conversion circuit of all parallel connected types, since the A/D converter of a configuration of changing by dividing into two, high order two or more bits and the remaining bits, can be used

TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] However, among the above-mentioned conventional A/D-conversion circuits, the thing of the former configuration has the problem that power consumption is size while a circuit scale becomes large since the comparator of about 1024 (= 210) individual and the partial pressure resistance for reference voltage generating are needed when it is going to output a 10-bit digital video signal.

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[0008] In for example, the case of a configuration of dividing into 6 bits of high orders and 4 bits of low order, and obtaining a digital signal output The property of an output digital signal over an input analog signal comes to be shown in drawing 4 , and although it is good since change of the quantization 1 Width of face from "0000001110" to "0000001111" is only change of 4 bits of low order, a 10-bit output Since the change of quantization 1 Width of face to "0000010000" from "0000001111" is change by the knot accompanied by change of 6 bits of high orders, and 4 bits of both low order, as A shows to this drawing, the problem of being inaccurate (distortion being large) has it.

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MEANS

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signal, and the A/D converter which changes the output signal of an adder circuit into a digital signal based on a sampling pulse.

OPERATION

[Function] In this invention, since analog-to-digital conversion is carried out by the A/D converter to an addition composite signal with the superposition signal of high frequency and he is trying to generate a digital signal rather than an input signal and this, change of digital value (sampling value) can be made small rather than it carries out direct analog-to-digital conversion to an input signal.
[0012] Moreover, a superposition signal can be reduced by having further the digital low pass filter which decreases a superposition signal component from the output digital signal of an A/D converter, and can acquire a desired digital signal

EXAMPLE

[Example] Next, the example of this invention is explained. Drawing 1 shows the block diagram of one example of this invention. Among this drawing, after the analog video signal inputted into the input terminal 1 is supplied to an adder circuit 2 and added with the superposition signal from the superposition signal generating circuit 3 here, it is supplied to A/D converter 4 and changed into a digital signal based on the sampling pulse from the sampling pulse generating circuit 6.
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supplied to the low pass filter 5 this digital signal of whose is a digital filter which is operating synchronizing with the sampling pulse from the sampling pulse generating circuit 6. It is low frequency from a superposition signal, and rather than the highest frequency of an input analog video signal, since cut-off frequency is set as 6MHz of a high frequency, it decreases a superposition signal by carrying out the passage output of the video-signal component as it is to an output terminal 7, and this digital low pass filter 5 is not outputted to an output terminal 7.

[0017] Drawing 2 shows an example of an input signal wave of A/D converter 4. As shown in this drawing, the superposition signal II from the above-mentioned superposition signal generating circuit 3 is compounded in an adder circuit 2 to the input video signal I which carries out the increment in monotone, and if the composite signal is sampled to the timing shown in drawing 2 by the arrow head by the above-mentioned sampling pulse in A/D converter 4, the sampling point will serve as a location shown in drawing 2 by the black dot. Therefore, also in the big input level of the quantization error of A/D converter 4, since it becomes the average with the level which the sampling value before and behind the level left for a while, a quantization error decreases.

[0018] Next, other examples of this invention are explained. Drawing 3 shows the block diagram of other examples of the A/D-conversion circuit which becomes this invention. The same sign is given to the same component as drawing 1 among this drawing, and the explanation is omitted. In drawing 3 , the analog video signal with a highest frequency of about 6MHz inputted from the input terminal 1 is supplied to adder 2a in an adder circuit 2 through the low pass filter (LPF) 10 whose cut-off frequency is 14MHz.

[0019] On the other hand, the sampling pulse generating circuit 12 is supplied to the superposition signal generating circuit 13 while it generates the 28.6MHz sampling pulse which synchronized with the synchronization pulse from an input terminal 11 and supplies this sampling pulse to A/D converter 4 and the digital low pass filter 14, respectively.

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superposition signal with the filter prepared in the D/A conversion circuit which follows. Moreover, a superposition signal may be the frequency of under 1 / 2 double of the frequency of a sampling pulse, and may be a frequency higher than the highest frequency of an input signal (you may not be a video signal).

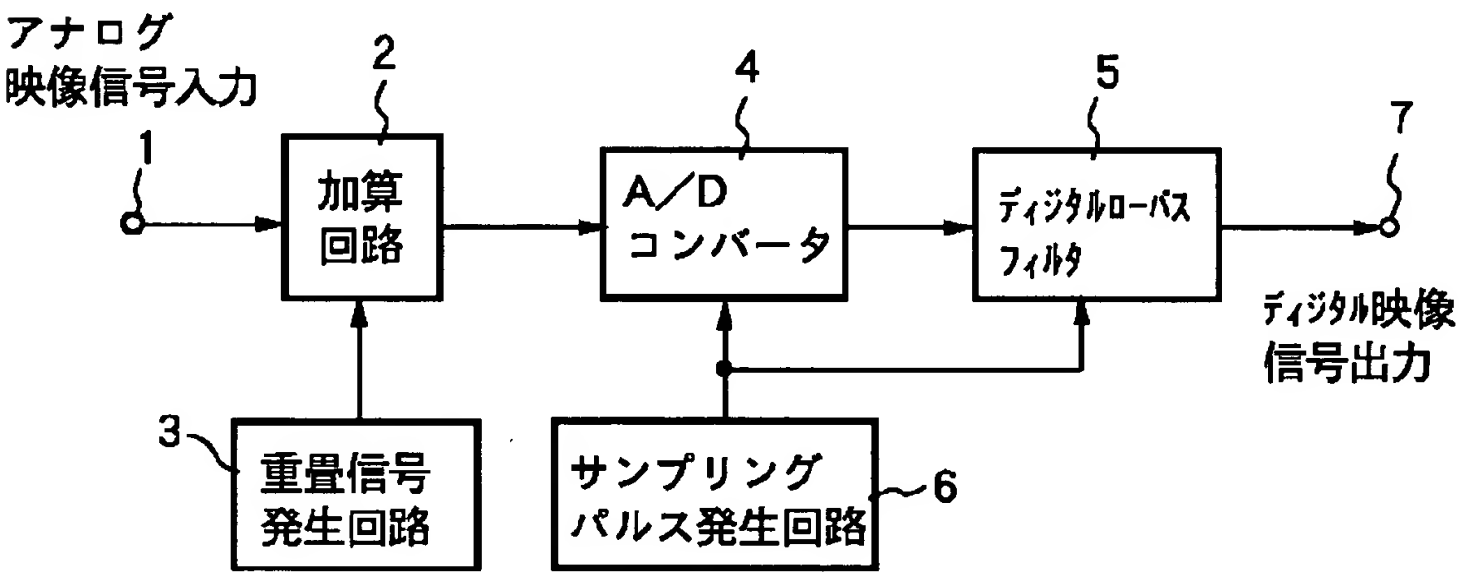
DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the block diagram of one example of this invention.
[Drawing 2] It is drawing showing an example of an input wave of the A/D converter of drawing 1 .
[Drawing 3] It is the block diagram of other examples of this invention.
[Drawing 4] It is drawing showing an example of the transfer characteristic of the conventional A/D-conversion circuit.

[Description of Notations]
1 Analog Video-Signal Input Terminal
2 Adder Circuit
3 13 Superposition signal generating circuit
4 A/D Converter
5 14 Digital low pass filter
6 12 Sampling pulse generating circuit
7 Digital Video-Signal Output Terminal
11 Synchronization Pulse Input Terminal

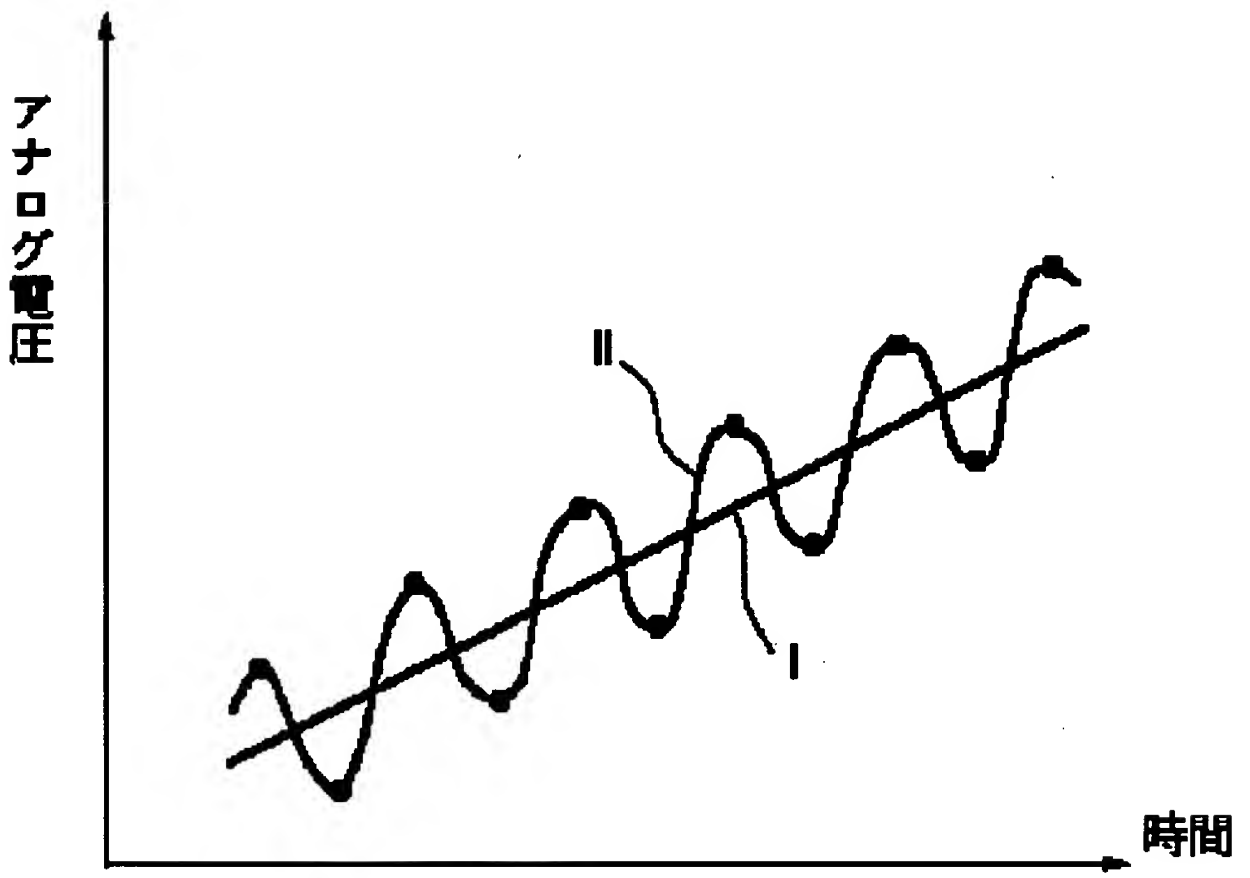
DRAWINGS

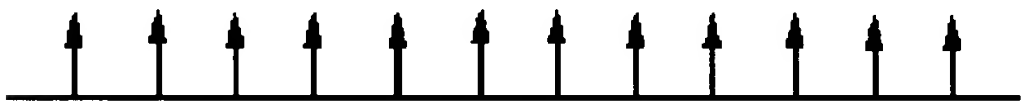
本発明の一実施例のブロック図



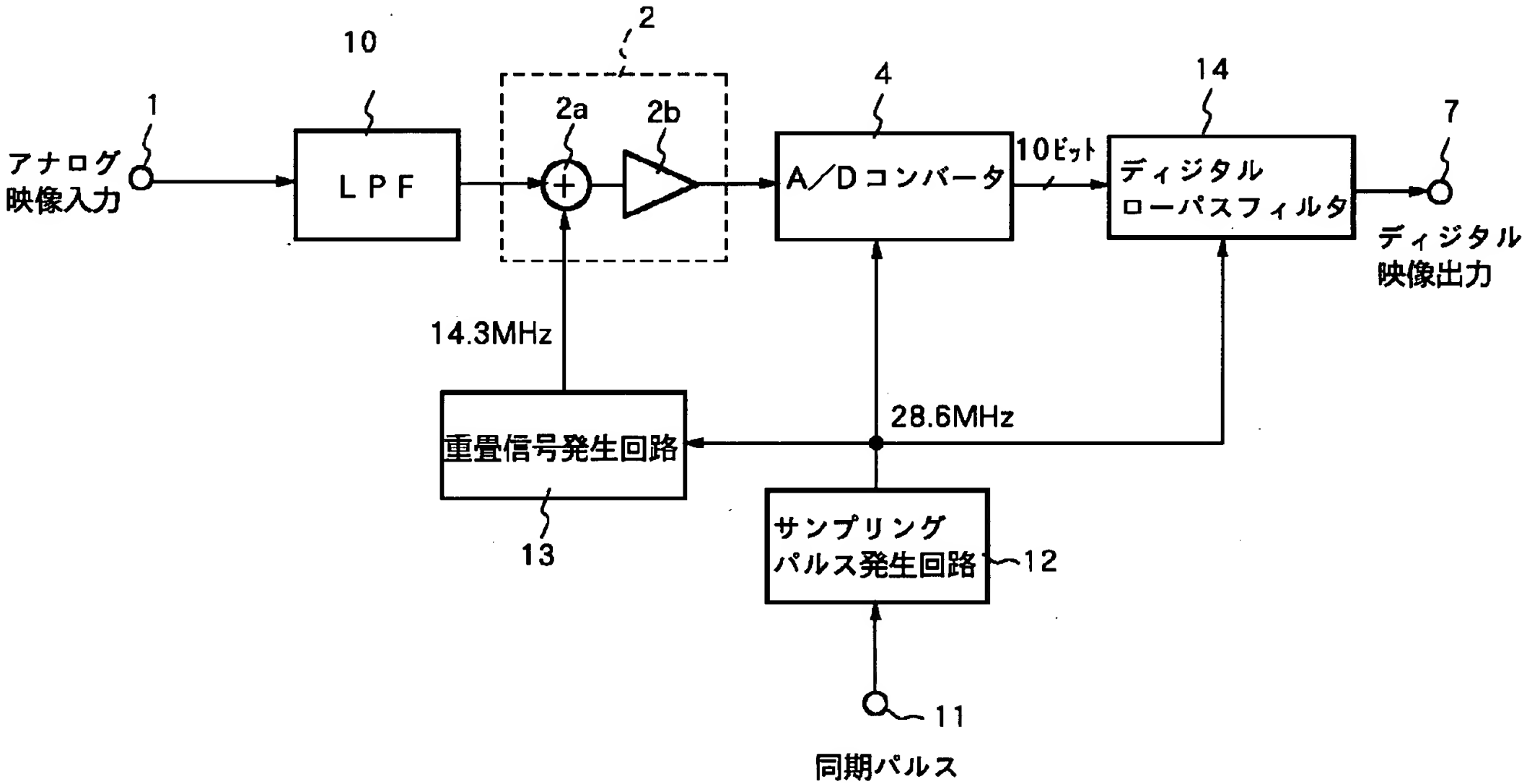
[Drawing 1]

図１のＡ／Ｄコンバータの入力波形の一例

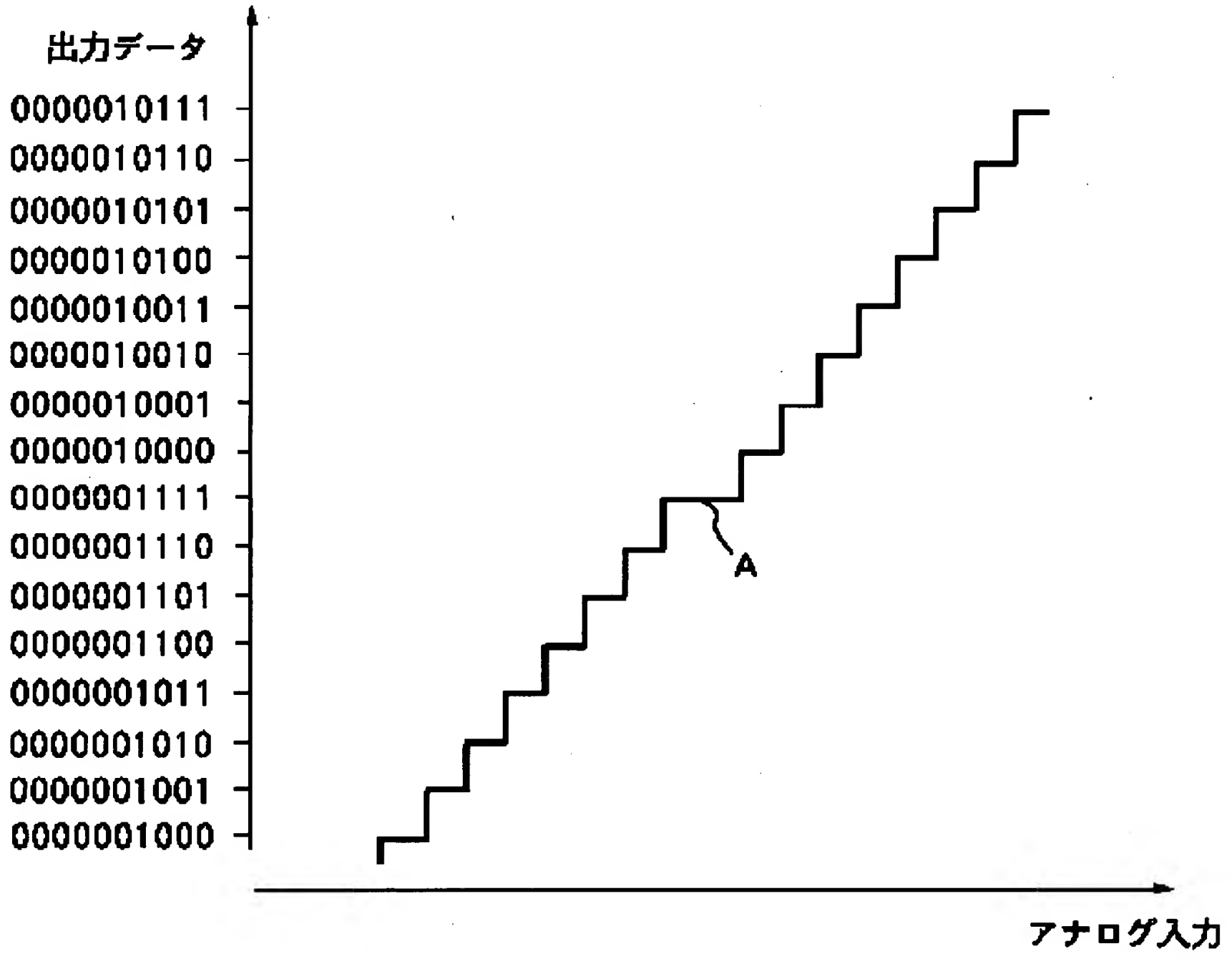




サンプリングパルス



本発明の他の実施例のブロック図



従来のA／D変換回路の変換特性の一例

(19)日本国特許庁（ＪＰ）　(12)**公開特許公報（A）**　(11)特許出願公開番号

特開平8－228152

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H03M	1/20			H03M	1/20	
	1/08				1/08	A

審査請求　有　請求項の数4　OL　（全 6 頁）

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東京都港区芝5丁目7番1号　日本電気株式会社内

(74)代理人　弁理士　松浦　兼行

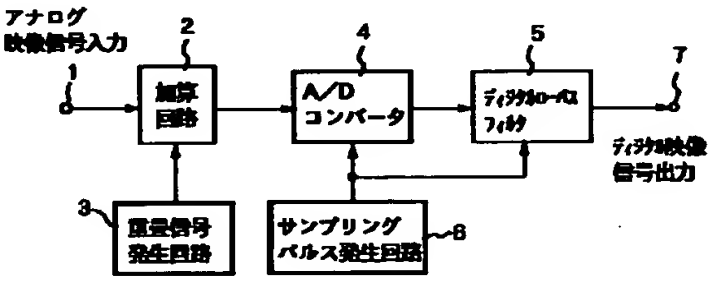
(54)【発明の名称】　A／D変換回路

(57)【要約】

【目的】　本発明は映像信号のように広周波数帯域の信号に対しても量子化誤差少なくアナログ・ディジタル変換し得るA／D変換回路を提供することを目的とする。

【構成】　サンプリングパルス発生回路6は、入力映像信号の最高周波数の2倍以上の周波数のサンプリングパルスを発生する。重畳信号発生回路3は、サンプリングパルスの1／2倍以下の周波数で、かつ、入力映像信号の最高周波数よりも高い周波数で一定振幅の重畳信号を発生し、加算回路2で入力映像信号に加算する。A／Dコンバータ4は、加算回路2の出力信号をサンプリングパルスに基づいてディジタル信号に変換する。ディジタルローパスフィルタ5は、A／Dコンバータ4の出力ディジタル信号から重畳信号成分を減衰して出力端子7へ出力する。

本発明の一実施例のブロック図



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【特許請求の範囲】
【請求項1】　入力信号の最高周波数の2倍以上の周波数のサンプリングパルスを発生するサンプリングパルス発生回路と、
該サンプリングパルスの1／2倍以下の周波数で、かつ、前記入力信号の最高周波数よりも高い周波数で一定振幅の重畳信号を発生する重畳信号発生回路と、
前記入力信号と前記重畳信号とを加算する加算回路と、該加算回路の出力信号を前記サンプリングパルスに基づいてディジタル信号に変換するA／Dコンバータとを有することを特徴とするA／D変換回路。
【請求項2】　前記A／Dコンバータは、入力信号を上位ビットと残りの下位ビットとの2つに分けてディジタル信号に変換する構成であることを特徴とする請求項1記載のA／D変換回路。
【請求項3】　A／Dコンバータの出力ディジタル信号から前記重畳信号成分を減衰するディジタルローパスフィルタを更に有することを特徴とする請求項1記載のA／D変換回路。
【請求項4】　前記重畳信号発生回路は、前記サンプリングパルスに基づいて該サンプリングパルスに同期した前記重畳信号を発生することを特徴とする請求項1乃至3のうちいずれか一項記載のA／D変換回路。
【発明の詳細な説明】
【0001】
【産業上の利用分野】本発明はA／D変換回路に係り、特に映像信号をアナログ・ディジタル変換するA／D変換回路に関する。
【0002】
【従来の技術】従来より、アナログ信号をディジタル信号に変換するA／D変換回路は広く用いられているが、映像信号をディジタル映像信号に変換するA／D変換回路は、映像信号の周波数帯域が比較的広帯域であるため、比較的高速度が要求される。このため、映像用A／D変換回路としては、従来全並列型のA／D変換回路知られている。
【0003】この全並列型のA／D変換回路は、Nビットの分解能を得る場合は（2^N-1）ビットのコンパレータと、この複数のコンパレータのそれぞれに入力映像信号と比較させるための互いに異なる基準電圧を発生させる複数の分圧抵抗と、複数のコンパレータの出力ディジタル信号をNビットのバイナリコードに変換するためのエンコーダとより構成され、入力映像信号を上記の複数のコンパレータにより対応する基準電圧と別々に、かつ、同時にレベル比較し、その比較結果をエンコーダを通すことにより出力ディジタル信号を得る。この全並列型のA／D変換回路は、高速であり、また微分的な1量子化の精度が比較的良好であるという特長がある。
【0004】また、従来の他のA／D変換回路としては、上位複数ビットと残りのビットの2つに分けて変換

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する、所謂2ステップフラッシュ型A／D変換回路が知られている。この従来のA／D変換回路は、上位複数ビット用の複数の第1のコンパレータと、下位ビット用の複数の第2のコンパレータと、互いに異なるレベルの参照電圧を第1及び第2のコンパレータに入力する参照電圧発生手段と、第1のコンパレータの出力結果に応じて第2のコンパレータに印加する参照電圧を切り換える切換手段と、第1及び第2のコンパレータの各出力をそれぞれ所定のビット数のディジタル信号に変換するエンコーダとよりなる。
【0005】この従来のA／D変換回路によれば、入力映像信号をそれぞれ複数の第1及び第2のコンパレータに並列に入力し、第一ステップで上位側の第1のコンパレータと参照電圧とを比較し、第二ステップで上記の比較結果に応じて下位側の第2のコンパレータへの参照電圧を切り換えて第2のコンパレータにより入力映像信号との比較を行う。そして、このようにして得られた第1及び第2のコンパレータの各比較出力をそれぞれ対応して設けられたエンコーダにより上位複数ビットのディジタル信号と、下位複数ビットのディジタル信号を得る。
【0006】
【発明が解決しようとする課題】しかるに、上記の従来のA／D変換回路のうち前者の構成のものは、10ビットのディジタル映像信号を出力しようとする場合は、約1024（$=2^{10}$）個のコンパレータと基準電圧発生用の分圧抵抗とを必要とするため、回路規模が大きくなると共に、消費電力が大であるという問題がある。
【0007】また、上記の従来のA／D変換回路のうち後者の構成のものは、コンパレータの数が少なく回路規模、消費電力が少なくて済む反面、上位のディジタル信号出力と下位のディジタル信号出力のつなぎ目での誤差が大きいという問題がある。
【0008】例えば、上位6ビットと下位4ビットに分けてディジタル信号出力を得る構成の場合、入力アナログ信号に対する出力ディジタル信号の特性は図4に示すようになり、10ビット出力が”0000001110”から”0000001111”への1量子化幅の変化は下位4ビットの変化だけであるため良好であるが、”0000001111”から”0000010000”への1量子化幅の変化は上位6ビットと下位4ビットの両方の変化を伴うつなぎ目での変化であるために同図にAで示すように精度が悪い（歪みが大きい）という問題がある。
【0009】本発明は以上の点に鑑みなされたもので、映像信号のように広周波数帯域の信号に対しても量子化誤差少なくアナログ・ディジタル変換し得るA／D変換回路を提供することを目的とする。
【0010】
【課題を解決するための手段】上記の目的を達成するため、本発明は、入力信号の最高周波数の2倍以上の周波

数のサンプリングパルスを発生するサンプリングパルス発生回路と、サンプリングパルスの１／２倍以下の周波数で、かつ、入力信号の最高周波数よりも高い周波数で一定振幅の重畳信号を発生する重畳信号発生回路と、入力信号と重畳信号とを加算する加算回路と、加算回路の出力信号をサンプリングパルスに基づいてディジタル信号に変換するA／Dコンバータとを有する構成としたものである。

【００１１】

【作用】本発明では、入力信号とこれよりも高周波数の重畳信号との加算合成信号に対してA／Dコンバータによりアナログ・ディジタル変換してディジタル信号を生成するようにしているため、入力信号に対して直接アナログ・ディジタル変換するよりもディジタル値（サンプリング値）の変化を小さくできる。

【００１２】また、重畳信号はA／Dコンバータの出力ディジタル信号から重畳信号成分を減衰するディジタルローパスフィルタを更に有することで低減でき、所望のディジタル信号を得ることができる。

【００１３】

【実施例】次に、本発明の実施例について説明する。図１は本発明の一実施例のブロック図を示す。同図中、入力端子１に入力されたアナログ映像信号は加算回路２に供給され、ここで重畳信号発生回路３よりの重畳信号と加算された後、A／Dコンバータ４に供給されてサンプリングパルス発生回路６よりのサンプリングパルスに基づいてディジタル信号に変換される。

【００１４】このA／Dコンバータ４は従来より公知の所謂２ステップフラッシュ型のA／Dコンバータであり、前記したように、第一ステップでは入力合成信号を上位ビット用の複数のコンパレータにおいて互いに異なる参照電圧と比較し、その比較結果に応じて第二ステップでは参照電圧を切り換えて下位ビット用の別の複数のコンパレータに印加し、この参照電圧と上記の入力合成信号とを比較し、以下同様の動作を繰り返す。そして、上記の上位ビット用の複数のコンパレータから取り出された各出力を上位ビット用のエンコーダを介して上位複数ビットのディジタル値を出力し、また、上記の下位ビット用の複数のコンパレータから取り出された各出力を下位ビット用のエンコーダを介して残りの下位複数ビットのディジタル値を出力する。

【００１５】ここで、サンプリングパルスの周波数は、ナイキストのサンプリング定理より通過させようとする入力アナログ映像信号の最高周波数の２倍以上の周波数であり、ここでは例えば入力アナログ映像信号の色副搬送波周波数の４倍の周波数である１４．３MHzである。また、上記重畳信号は、このサンプリングパルスの周波数の１／２倍の周波数の正弦波で、振幅は１量子化幅の５倍程度である。

【００１６】このようにして、A／Dコンバータ４から

は映像信号と重畳信号との合成信号が上位ビットと下位ビットの２つに分けてディジタル信号に変換され、全体として量子化ビット数が例えば１０ビットで取り出され、このディジタル信号はサンプリングパルス発生回路６よりのサンプリングパルスに同期して動作しているディジタルフィルタであるローパスフィルタ５に供給される。このディジタルローパスフィルタ５は、遮断周波数が重畳信号よりも低周波数で、かつ、入力アナログ映像信号の最高周波数よりも高い周波数の例えば６MHzに設定されているため、映像信号成分はそのまま出力端子７へ通過出力され、重畳信号は減衰されて出力端子７へ出力されない。

【００１７】図２はA／Dコンバータ４の入力信号波形の一例を示す。同図に示すように、例えば単調増加する入力映像信号Ｉに対して上記の重畳信号発生回路３よりの重畳信号ＩＩが加算回路２で合成され、その合成信号がA／Dコンバータ４において上記サンプリングパルスにより図２に矢印で示すタイミングでサンプリングされると、そのサンプリング点は図２に黒丸で示す位置となる。よって、A／Dコンバータ４の量子化誤差の大きな入力レベルにおいても、そのレベルの前後のサンプリング値が少し離れたレベルとの平均値となるので、量子化誤差が低減する。

【００１８】次に、本発明の他の実施例について説明する。図３は本発明になるA／D変換回路の他の実施例のブロック図を示す。同図中、図１と同一構成部分には同一符号を付し、その説明を省略する。図３において、入力端子１より入力された最高周波数６MHz程度のアナログ映像信号は、遮断周波数が１４MHzのローパスフィルタ（ＬＰＦ）１０を介して加算回路２内の加算器２ａに供給される。

【００１９】一方、サンプリングパルス発生回路１２は入力端子１１よりの同期パルスに同期した２８．６MHzのサンプリングパルスを発生し、このサンプリングパルスをA／Dコンバータ４及びディジタルローパスフィルタ１４にそれぞれ供給すると共に、重畳信号発生回路１３に供給する。

【００２０】重畳信号発生回路１３は入力サンプリングパルスに同期した１／２倍の周波数の１４．３MHzで、かつ、振幅が前記したように５量子化幅程度の重畳信号を発生して加算器２ａに供給し、ここでＬＰＦ１０よりのアナログ映像信号と加算させる。

【００２１】この加算器２ａより取り出されたアナログ映像信号と重畳信号との合成信号は、増幅器２ｂで増幅された後、A／Dコンバータ４に供給されて２８．６MHzのサンプリングパルスによりオーバーサンプリングされて、例えば量子化ビット数１０ビットのディジタル信号に変換される。このディジタル信号は通過帯域が約６MHzのディジタルローパスフィルタ１４により、映像信号成分がそのまま通過されて出力端子７へ出力さ

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れ、重畳信号成分は減衰される。本実施例は、重畳信号がサンプリングパルスに同期しているので、重畳信号の山と谷の部分をそれぞれ正確にサンプリングでき、また、オーバーサンプリングしているのでより正確で量子化誤差の少ないディジタル信号に変換できる。

【００２２】なお、本発明は上記の実施例に限定されるものではなく、例えば実施例では重畳信号減衰のためのディジタルローパスフィルタ５、１４をA／D変換回路内に設けたが、後続するD／A変換回路内に設けられたフィルタで重畳信号を減衰させることも可能である。また、重畳信号はサンプリングパルスの周波数の１／２倍未満の周波数で、かつ、入力信号（映像信号でなくてもよい）の最高周波数よりも高い周波数であってもよい。

【００２３】

【発明の効果】以上説明したように、本発明によれば、入力信号とこれよりも高周波数の重畳信号との加算合成信号に対してA／Dコンバータによりアナログ・ディジタル変換してディジタル信号を生成することにより、入力信号に対して直接アナログ・ディジタル変換するよりもディジタル値（サンプリング値）の変化を小さくできるため、従来に比べて微分的な量子化誤差を低減したディジタル信号を得ることができ、よって、上位複数ビットと残りのビットの２つに分けて変換する構成のA／Dコンバータを使用できるために、全並列型のA／D変換回路に比べて回路規模を低減できると共に、消費電力も低減できる。

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【図面の簡単な説明】

【図１】本発明の一実施例のブロック図である。

【図２】図１のA／Dコンバータの入力波形の一例を示す図である。

【図３】本発明の他の実施例のブロック図である。

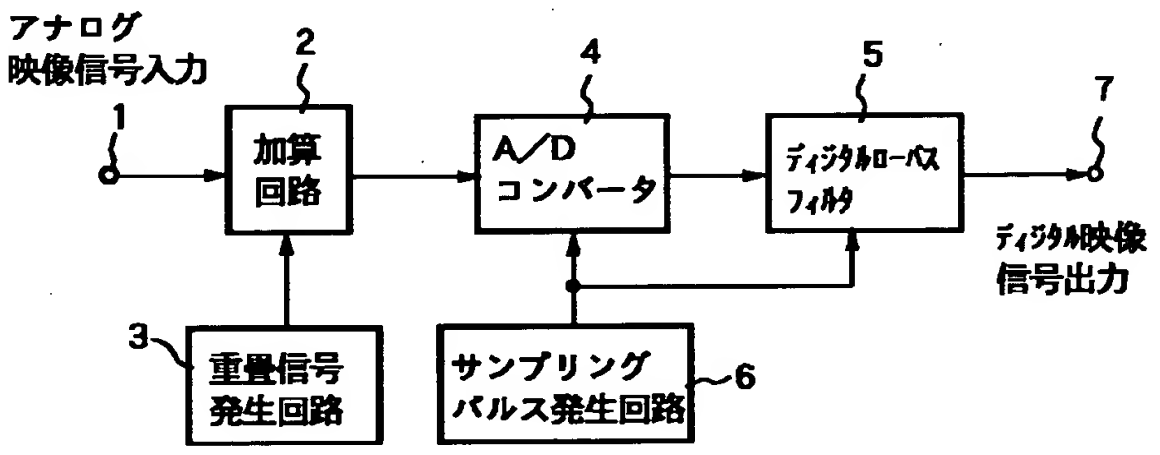
【図４】従来のA／D変換回路の変換特性の一例を示す図である。

【符号の説明】

１　アナログ映像信号入力端子
２　加算回路
３、１３　重畳信号発生回路
４　A／Dコンバータ
５、１４　ディジタルローパスフィルタ
６、１２　サンプリングパルス発生回路
７　ディジタル映像信号出力端子
１１　同期パルス入力端子

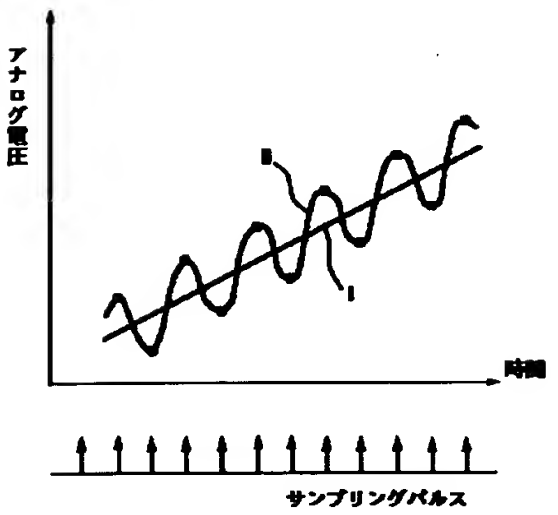
【図１】

本発明の一実施例のブロック図



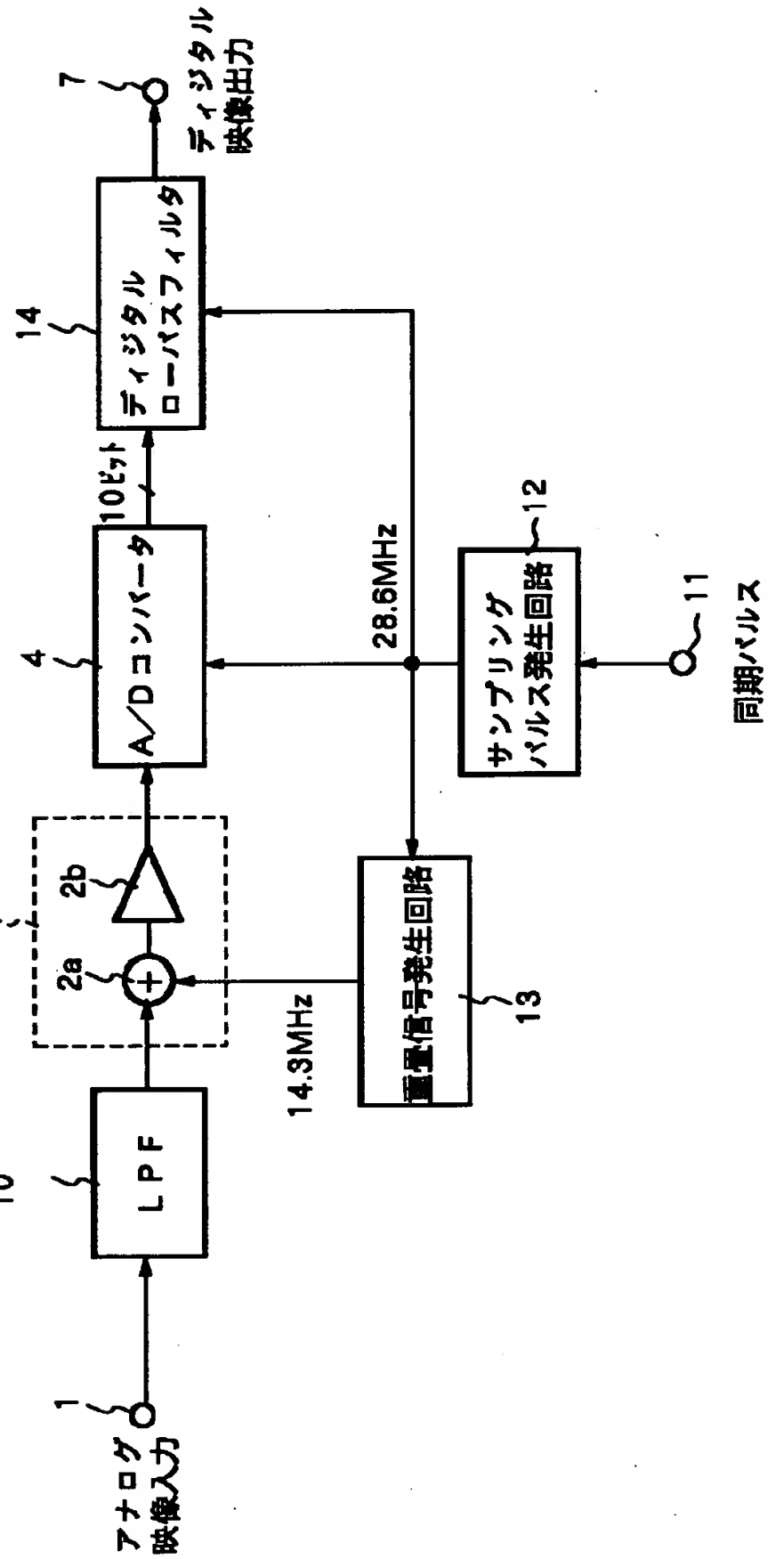
【図2】

図1のA/Dコンバータの入力波形の一例

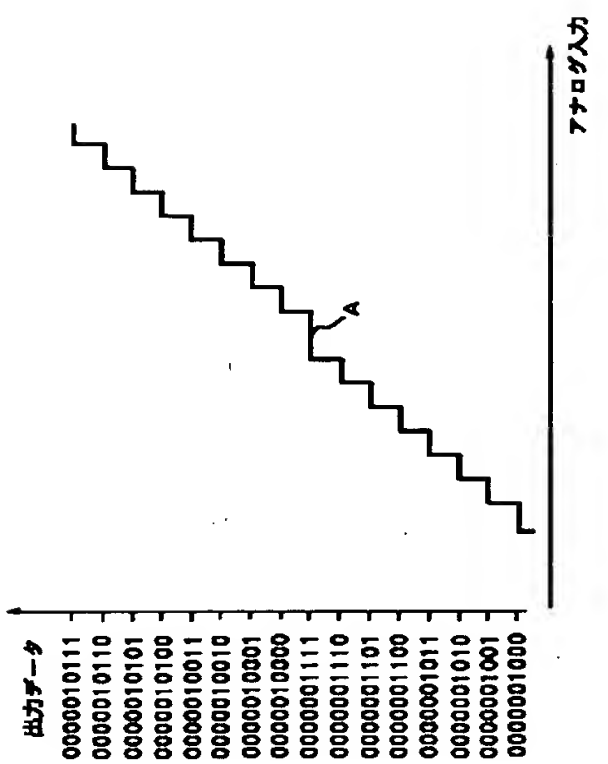


【図3】

本発明の他の実施例のブロック図



【図4】


従来のA/D変換回路の変換特性の一例
アナログ入力
出力データ
0000010111
0000010110
0000010101
0000010100
0000010011
0000010010
0000010001
0000010000
0000001111
0000001110
0000001101
0000001100
0000001011
0000001010
0000001001
0000001000